General Principles in Heat Sink Selection for Xilinx All-Programmable FPGAs, 3D ICs and SoCs

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The reliability and performance of electronic devices require proper thermal management design. For the Xilinx All-Programmable FPGA, 3D IC and SoC product lines, the subject is somewhat complex due to two factors: (1) the amount of heat generated is largely dependent upon the utilization of a particular IC configuration in the customer application and (2) the variety of different packages offered.

Power and cooling specifications for All-Programmable SoC and FPGA designs have to be determined early in the product’s design cycle. An accurate worst-case power analysis early on helps users avoid the pitfalls of overdesigning or under-designing your product’s power or cooling system. Xilinx developed the Xilinx Power Estimator (XPE) for this purpose. XPE estimates the power consumption of your design at any stage during the design cycle. It accepts design information through simple design wizards, analyzes them and provides a detailed power and thermal information.

Xilinx also provides a Package Thermal Data Query tool. It allows users to input the device family (for example Virtex®-7), device name (for example XC7V585T) and package code (for example FF1157) to obtain product specific thermal data. The results of the query include the thermal resistances $\theta_{JA}$ (still air up to 750 LFM), $\theta_{JB}$ and $\theta_{JC}$ per EIA-JESD51 methods. The result of the above example is as shown:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\theta_{JA}$ (Still Air)</td>
<td>8.7 °C/W</td>
</tr>
<tr>
<td>$\theta_{JA}$ (250 LFM)</td>
<td>5.6 °C/W</td>
</tr>
<tr>
<td>$\theta_{JA}$ (500 LFM)</td>
<td>4.8 °C/W</td>
</tr>
<tr>
<td>$\theta_{JA}$ (750 LFM)</td>
<td>4.3 °C/W</td>
</tr>
<tr>
<td>$\theta_{JB}$</td>
<td>2.3 °C/W</td>
</tr>
<tr>
<td>$\theta_{JC}$</td>
<td>0.14 °C/W</td>
</tr>
</tbody>
</table>

Proper thermal design is generally dependent on the heat sink utilized, the airflow and the thermal interface material (TIM) used to enable efficient transfer of the power dissipated by the integrated circuit (IC) to the heat sink. CTS Electronic Components (CTS), a leading manufacturer of advanced thermal solutions, offers a high-performance, general-use, peel-and-stick thermal adhesive tape, type A01, which has the advantages of ease-of-use and high performance. Several other standard TIM tapes and clip options for efficient and robust mounting are available. Figure 1 below shows a typical attachment structure for a Flipchip/BGA IC:
Figure 2 shows an example of the primary heat transfer paths for an IC with an attached heat sink mounted to a printed circuit board:

![Heat Transfer Paths Diagram]

Virtually all of the heat generated in the device is removed by the heat sink. Heat is conducted through the silicon or plastic, through the TIM and to the heat sink. The IC junction-to-case ($\theta_{JC}$) thermal resistance is low enough such that the TIM thermal impedance and heat sink thermal resistance are the dominant terms.

A simple approach for heat sink selection with a specific thermal resistance assumes that all generated heat flows serially from the semiconductor transistor junction to the case, then across the TIM into the heat sink and is finally dissipated from the heat sink to the air stream. This approach works for many applications and requires only basic calculations. Here are some questions to consider before selecting a thermal management solution:

- What is the ambient temperature of the application?
- What is the junction temperature of the semiconductor?
- What heat is produced by the semiconductor?
- What is junction-to-case thermal resistance of the semiconductor?
- What thermal resistance of the TIM?
- What is the size of the semiconductor?

If these basic questions can be answered, a heat sink can be found for almost any application. How can these be answered?

- Ambient temperature ($T_A$) is often a design parameter.
- Junction temperature ($T_J$) can be measured or calculated.
- Total heat produced by the semiconductor ($Q$) can be calculated.
- Junction-to-case thermal resistance ($\theta_{JC}$) is provided in semiconductor data sheets.
- Thermal resistance of the TIM ($\theta_{CS}$) is provided by the material manufacturers.
Many assume calculating the junction-to-ambient thermal resistance ($\theta_{JA}$) is just the thermal resistance of the heat sink itself. However, as illustrated in Figure 3, $\theta_{JA}$ is a combination of three specific thermal resistances:

- Junction to Case Thermal Resistance ($\theta_{JC}$)
- Case to Surface Thermal Resistance ($\theta_{CS}$)
- Surface to Ambient Thermal Resistance ($\theta_{SA}$)

Given the following equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

Eq. 1.

$\theta_{JA}$ can also be calculated as the difference between ambient temperature and junction temperature divided by the total heat given off by the semiconductor.

$$\theta_{JA} = \frac{(T_J - T_A)}{Q}$$

Eq. 2

The thermal resistance needed for appropriate heat sink selection is calculated by combining equations 1 and 2 and solving for $\theta_{SA}$.

$$\theta_{SA} = \frac{(T_J - T_A)}{Q} - \theta_{CS} - \theta_{JC}$$

Eq. 3.
Let's look at a design example using a typical Xilinx FPGA. $T_j$ is measurable using internal temperature sensing on the FPGA. $T_A$, $Q$, $\theta_{JC}$ and $\theta_{CS}$ are all known quantities.

\[
\begin{align*}
T_j &= 85 \, ^\circ C \\
T_A &= 22.4 \, ^\circ C \\
Q &= 2.232 \, W \\
\theta_{CS} &= 1 \, ^\circ C/W \\
\theta_{JC} &= 3.92 \, ^\circ C/W \\
\theta_{SA} &= 24.02 \, ^\circ C/W
\end{align*}
\]

This calculated $\theta_{SA}$ represents the maximum thermal resistance a heat sink should have to dissipate heat effectively in the given application. Selection of the appropriate heat sink depends on many other factors. These include thermal performance at a given airflow rate, pressure drop, spatial volume, mass, attachment method and cost. Due to the variety of packages and IC thicknesses offered by Xilinx, CTS offers a variety of heat sink sizes, clipping options and TIMs for use with most Xilinx devices.

The CTS Heat Sink Selector Guide for Xilinx All-Programmable FPGAs, 3D ICs and SoCs recommends appropriately sized heat sinks for most Xilinx IC packages. It documents how to build the correct part number to select appropriate TIM and mounting options. Contact your local CTS Manufacturer's Representative or Avnet Account Manager or FAE for support in choosing the right heat sink and mounting options for your specific application. For more information about pricing, availability and technical information on all of these thermal relief solutions, please visit www.em.avnet.com/ctsheatsinks.
ABOUT THE AUTHORS

The CTS Thermal Solutions Team is a group of dedicated and highly competent engineers that continues on a path set generations ago; to offer innovative products and services that meet the specialized and changing needs of its customers.

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